10015055-1

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Daniel J. Dove
Serial No.:	09/939,418
Conf. No.:	4205
Filed:	08/24/2001
For:	REDUCED PIN-COUNT SYSTEM INTERFACE FOR GIGABIT ETHERNET PHYSICAL LAYER DEVICES
Art Unit:	2665
Examiner:	Khuong, Lee T.

I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

6/28/05 *Roger D. Greer*

Date *Registration No.* 26,174

F-CLASS.WCM
Appr. February 20, 1998 *Attorney for Applicant(s)*

DECLARATION OF ROGER D. GREER OF PRIOR INVENTION TO OVERCOME CITED PUBLICATION (37 C.F.R. §1.131)

1. I am an attorney of record for the above-identified patent application.

2. The above-referenced patent application was prepared by me in the offices of Greer, Burns & Crain, Ltd. of which I am a principal.

3. In a letter dated April 26, 2001 to me from Mr. David M. Mason, a Senior Patent Agent with Hewlett-Packard Company, Mr. Mason requested that I provide a quote for the cost to prepare a patent application for the above-referenced patent application. A copy of the April 26, 2001 letter is attached hereto as Exhibit A.

4. One of the enclosures to the April 26, 2001 letter was a document entitled "Reduced Gigabit Media Independent Interface (RGMII)" which is dated September 22, 2000. The RGMII document has seven pages of drawings and text that describe the invention in detail. A copy of the RGMII September 22, 2000 document is attached as Exhibit B.

5. The RGMII document clearly demonstrates that the invention was completed well prior to the filing date of May 30, 2001 of the Chadha et al. 6,604,206 patent that the examiner has cited as the basis for a §102(e) rejection of all claims in the above-referenced patent application. The Chadha patent is not prior art to applicant's claimed invention.

6. Responsive to Mr. Mason's request in his letter and to the written Request for Quote and Engagement Letter Agreement, which was another enclosure in his letter, the undersigned prepared a proposal for the preparation of a patent application and faxed it to Mr. Mason on June 8, 2001, which was signed and returned on the same date. A copy of that document is attached as Exhibit C.

7. I then began preparing the application and had discussions with the inventor Mr. Dove by telephone where we used Exhibit B as the subject of the discussions.

8. On July 17, 2001, I sent an email to Mr. Mason and Mr. Dove which included revised drawings. A copy of the email is attached as Exhibit E.

9. Upon completion of the application in early August, 2001, I sent it to Mr. Mason and Mr. Dove, and received an email from Mr. Dove with his comments on August 20, 2001. A copy of the email is attached as Exhibit D. Mr. Dove indicated that he was sorry it took so long to review the application, because he had been working on what he called "hot-sites" for the previous week and a half.

10. The changes were made to the application and it was filed August 24, 2001.

11. As a person signing below, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under 18 U.S.C. §1001, and that such willful statements may jeopardize the validity of this application or any patent issued thereon.

Dated: 6/28/05

Roger D. Greer

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April 26, 2001

Mr. Roger D. Greer
Greer, Burns & Crain Ltd.
300 S. Wacker Drive
25th Floor
Chicago, IL 60606

RE: Request for Quote
HP PDNO: 10015055-1
Title: A Reduced System Interface For 10/100/1000 Megabit Per Second Network Integrated Circuits
Inventor(s): Daniel J. Dove

Dear Roger:

Please give us a quote of the cost to perform the services indicated on the attached *Request For Quote And Engagement Letter Agreement* (hereinafter "RFQ") form, for the above-identified matter, pursuant to Outside Counsel Procedures revised October 15, 1999, a copy of which you have received and reviewed. The quote should be based on your preparing and providing the requested services by the date for receipt by HP and/or the USPTO as indicated.

Your quote should be submitted on the enclosed RFQ form. If we accept your quote, we will return a fully executed copy of the Agreement to you for your records. **The Agreement will not be binding on you or on HP until signed by HP's authorized representatives.**

If the Agreement is not signed and returned to HP, any bills submitted by you cannot be paid.

Thank you for your assistance. If performing these services might involve a possible conflict of interest for your firm, you should advise us within one week of receipt of this letter.

Sincerely,

David M. Mason
Senior Patent Agent

DMM/tf

Enclosure(s)

Exhibit A

Your Logo Here!

Your Logo Here!

Reduced Gigabit Media Independent Interface (RGMII)

9/22/2000
Version 1.2a

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	Sept 11, 2000	a) Changed TD[4]/TXEN_TXERR signal name to TX_CTL b) Changed RD[4]/RXEN_RXERR signal name to RX_CTL c) Removed 100ps jitter requirement from TXC d) Changed RXC derivation to received data stream e) Clarified Table 1 description of TX_CTL and RX_CTL logical functions f) Required CRS assertion/deassertion to be synchronous for all speeds. g) Returned timing numbers to absolute from percentages. h) Relaxed 10/100 Duty cycle requirements to 40/60 i) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. j) Modified Table 4 to incorporate optional in-band signaling of link status, speed, and duplex. k) Slight wording change on IP statements to limit scope and indemnify.
1.2a	Sept 22, 2000	a) Clarified 3.4.2 statement to eliminate suggestion that in-band status was only required for half-duplex. b) Modified Table 2 to from "Clock to Data skew" to "Data to Clock skew" to clarify the fact that clock is delayed relative to data. c) Modified section 4.0 to clarify that MDIO/MDC are also operating at 2.5v CMOS levels.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

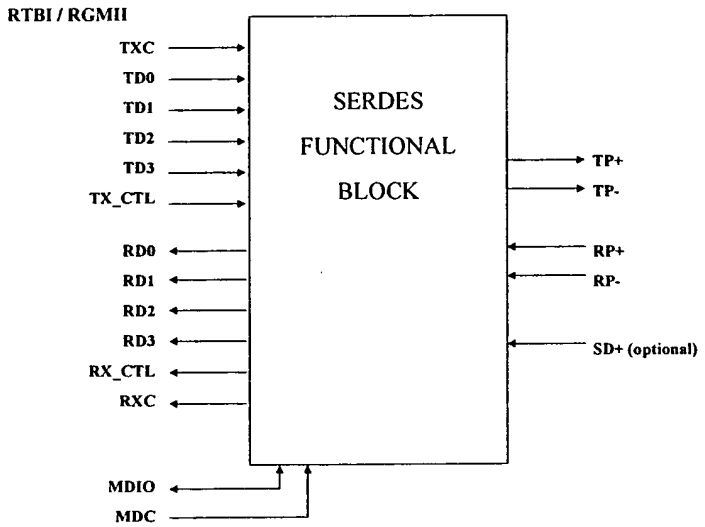

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm depending on speed.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TX_CTL	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, and a logical derivative of TXEN and TXERR on ↓ of TXC as described in section 3.4
RXC	PHY	PHY	The continuous receive reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm. and shall be derived from the received data stream
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RX_CTL	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, and a derivative of RXDV and RXERR on ↓ of RXC as described in section 3.4

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than VOH_MIN, and logic "low" when it is at a valid voltage level less than VOL_MAX.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

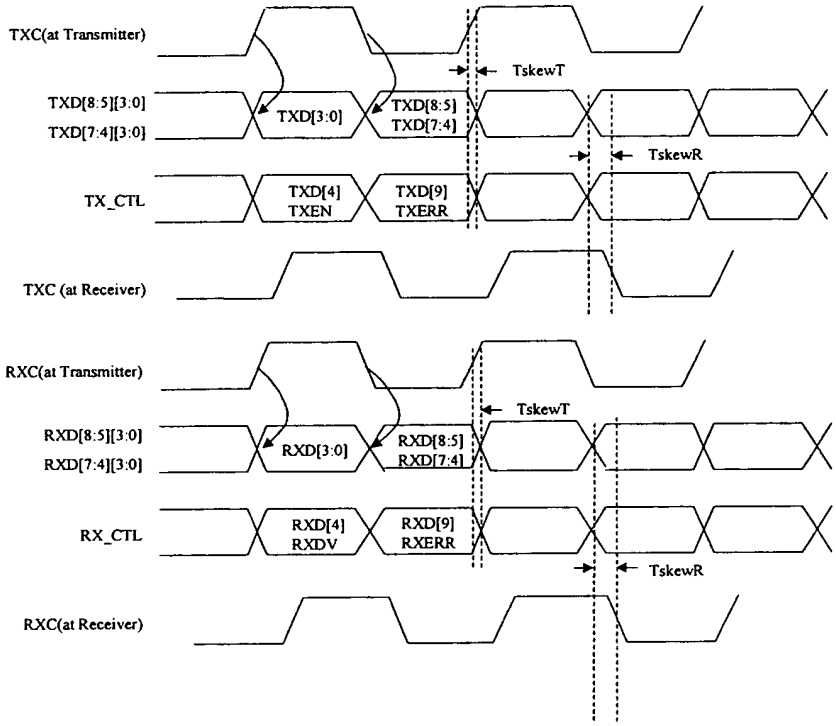

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at Receiver) *note 1	1		2.8	ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit *note 3	45	50	55	%
Duty_T	Duty Cycle for 10/100T *note 3	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.

note 3: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

TABLE 2

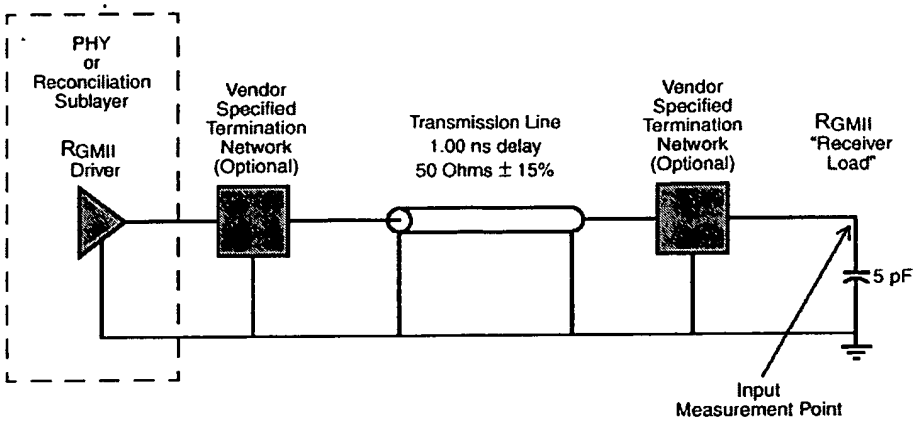

FIGURE 3

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0,0	0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0,1	0	1	00 through 0E	Reserved —	
0,1	0	1	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	10 through 1E	Reserved —	
0,1	0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0,1	0	1	20 through FE	Reserved —	
1,1	1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1,0	1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

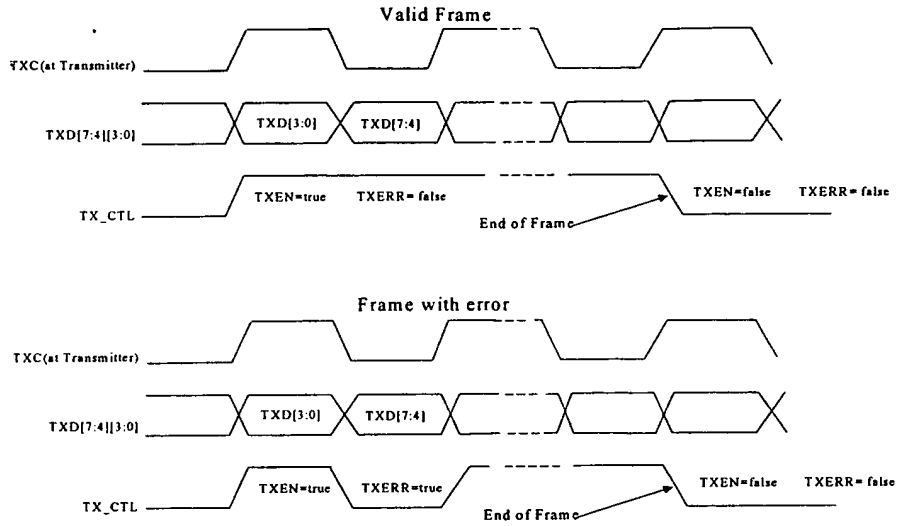

FIGURE 4

RX_CTL	GMII_RX_DV	GMII_RX_ER		RXD[7:0]	Description	PLS_DATA.indicate or PHY_ status parameter
0,0	0	0	#	xxx1 or xxx0	Normal inter-frame	Indicates link status 0=down, 1=up
0,0	0	0	#	x00x or x01x x10x or x11x	Normal inter-frame	Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved
0,0	0	0	#	1xxx or 0xxx	Normal inter-frame	Indicates duplex status 0=half-duplex, 1=full duplex
0,1	0	1	*	00	Reserved	—
0,1	0	1	*	01through 0D	Reserved	—
0,1	0	1	*	0E	False Carrier indication	False Carrier Present
0,1	0	1	*	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	*	10 through 1E	Reserved	—
0,1	0	1	*	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0,1	0	1	*	20 through FE	Reserved	—
0,1	0	1	*	FF	Carrier Sense	PLS_Carrier.Indicate
1,1	1	0	*	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1,0	1	1	*	00 through FF	Data reception error	ZERO, ONE(eight bits)

* NOTE— (Required Function) Values in RXD[7:0] column are in hexadecimal.
\# NOTE— (Optional) Values in RXD[7:0] column are in binary; nibbles are repeated on ↑ edge and ↓ edge.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

3.4.1 In-Band Status (Optional)

In order to ease detection of the link status, speed and duplex mode of the PHY, inter-frame signals will be placed onto the RXD[3:0] signals as indicated in table 4. The status of the PHY shall be indicated whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, or False Carrier are not present. When link status is down, PHY speed and duplex are defined by the PHY's internal setting.

3.4.2 In-Band Status (Required)

CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring as defined in Table 4. Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only.

Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

4.0 Electrical Characteristics

The RGMII and RTBI signals (including MDIO/MDC) will be based upon 2.5v CMOS interface voltages as defined by JEDEC EIA/JESD8-5.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.0	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH}_Min; V_{CC}=Min	1.7	–	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL}_Max; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	uA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	uA

TABLE 5

5.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks are allowed during speed transitions.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the ↓ edge of the appropriate clock.

The MAC will hold TX_CTL low until it has ensured that it is operating at the same speed as the PHY.

6.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

7.0 Hewlett Packard Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document for the express purpose of implementation of this specification to encourage others to adopt this interface as an industry standard. Any company wishing to use this specification may do so if they will in turn relinquish their proprietary rights to information contained or referenced herein. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

7.1 Contributions of Intellectual Property

All contributing companies incorporating their logo on this document have relinquished their proprietary rights to information contained in this document for the express purpose of implementation of this specification to encourage others to adopt this interface as an industry standard. Any questions concerning their contributions should be directed to their corporate headquarters.

7.2 Disclaimer

This RGMII Specification is provided "as is" with no warranties whatsoever, including any warranty of merchantability, non-infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification, or sample.

All contributing companies incorporating their logo on this document disclaim all liability for infringement of proprietary rights, relating to use of information in this specification.

Request for Quote and Engagement Letter Agreement

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___ This is a confirmation of your quote for the following services:

PREPARE

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___ Response
___ Other _____

X File with USPTO
___ Return to HP for filing

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HP REQUIRED DATES:

_____ Date for Receipt by HP
6/15/01 Date to be Filed in PTO

HP Attorneys of Record: (to be included on the Declaration)

Customer Number 022879

HP Primary Technical Contact: Daniel Dove

Telephone No.: (916) 785-4187 **FAX No.:**

HP Entity: IIPS

Address: 8000 Foothills Blvd., MS 5555
Roseville, CA 95747

ADDITIONAL TERMS OR INSTRUCTIONS:

RELATED TO: 10981938-2; Your Ref.: 3417.64843
S/N: 09/691,726

A copy of the filing receipt is enclosed. Also enclosed is the issued patent of the parent.

TOTAL PRICE: _____ **(including Formal drawings)**

I agree to the terms of this Agreement including the additional terms above, pursuant to the HP Procedures for Outside Counsel revised **OCTOBER 15, 1999** a copy of which I have received and reviewed. This Agreement will not be binding on either party until signed by an authorized representative of HP.

GREER, BURNS & CRAIN LTD.

By: _____
Roger D. Greer

Dated: 6/8/01

HEWLETT-PACKARD COMPANY

By: _____
David M. Mason

Dated: 6/8/01

Exhibit C

Roger D. Greer

From: DOVE,DANIEL J (HP-Roseville,ex1) [dan_dove@hp.com]
Sent: Monday, August 20, 2001 2:35 PM
To: 'Roger D. Greer'; DOVE,DANIEL J (HP-Roseville,ex1)
Cc: MASON,DAVE (HP-Cupertino,ex1)
Subject: RE: 10115055-1 patent drawings.

Hi Roger,

Sorry for taking so long to review the patent app, but I have been working on what we call "hot-sites" for the last week and a half.

6560?
6?326

Here are my comments;

Page 2 - line 4: change "BMII" to "GMII".

Page 2 - line 5: remove the hyphen in "Gigabit"

Page 2 - line 16: Add "A novel selection of signal assignments optimizes this interface beyond any obvious selection. For example, assigning CRS and COL together allows gigabit implementations which are typically full-duplex to eliminate an additional pin.

Page 5 - line 3: Change "the lower three bits" to "the lower four bits".

Page 7 - Line 7: Add "which is easier to implement in an integrated circuit than fixed delay offsets.

Page 11 - You might want to reiterate a statement about the value of assigning CRS/COL to a single line so that it can be eliminated for gigabit only implementations.

Figure 2
- Change TXF[B-5] to TXD[8:5]
- Put TXEN above TXD4 on the next line.
- Add RXD[8:5] below RXD[7:4] in next figure down.
- Behind RGMII, put RXDV_RXERR on the next line of the lower figure
- Behind RTBI put RXD4_RXD9
- Modify the value in the cell from just RXDV to RXDV with RXD4 below it.
- Modify the value in the cell from just RXERR to RXERR with RXD9 below it.

If there are any questions, feel free to call.

Regards,

Dan

Daniel Dove Principal Engineer
dan_dove@hp.com LAN PHY Technology

Exhibit D

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Fax : 916 785 1815
Invent!

> -----Original Message-----
> From: Roger D. Greer [mailto:rgreer@gbclaw.net]
> Sent: Tuesday, July 17, 2001 1:12 PM
> To: Dan Dove (E-mail)
> Cc: Dave Mason (E-mail)
> Subject: 10115055-1 patent drawings.
>
>
> Dan,
> Here are slightly revised drawings, particularly FIG. 2.
>
> Regards,
> Roger D. Greer
> Greer, Burns & Crain, Ltd.
> Suite 2500
> 300 South Wacker Dr.
> Chicago, IL 60606
> 312 360-0080
> Fax 312 360-9315
> Direct line 312 987-4000
>
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Exhibit E